



QSFP+ SR4 Active Optical Cable(QSFP+ AOC)

Compliance with the 40GBASE-SR4 of the IEEE 802.3ba standard.

Supports 40 Gbps data rate links of up to 100m



Description

APAC QSFP+ Active Optical Cable (AOC) product is a new high speed pluggable I/O interface products. This interconnecting module offers 4 channels and maximum bandwidth of 40Gbps. This module provides high performance and excellent efficiency in the optical communication.

Features

- Compliant with 40G Ethernet IEEE 802.3ba 40GBASE-SR4 standards
- QSFP footprint (Quad small form-factor, pluggable)
- Compliant with QDR/DDR/SDR Infiniband data rates
- Hot pluggable electrical interface
- RoHS-6 Compliant (lead-free)

Application

- 40GBASE-SR4 Ethernet links
- Infiniband QDR, DDR & SDR interconnects
- Client-side 40G Telecom connections

Ordering information

PART NUMBER	DESCRIPTION	NOTE
LM2C-K3D-TC-N- <u>XX</u>		Round type cable
	<u>XX</u> : Cable Length	
	01: 1m 03: 3m 05:5m A0:100m	
	10: 10m 40: 40m 70:70m	
	20: 20m 50: 50m 80:80m	
	30: 30m 60: 60m 90:90m	



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Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

PARAMETER	MIN	MAX	UNITS	NOTE
Storage Temperature	-10	70	°C	
3.3V Power Supply Voltage	-0.5	3.6	V	
Data Input Voltage- Single Ended	-0.5	V _{cc} +0.5	V	
Control Input Voltage	-0.5	3.6	V	
Relative Humidity	5	85	%	

Recommend Operating Condition

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Case Temperature	T _c	0	40	70	°C	
3.3V Power Supply Voltage	V _{cc}	3.15	3.3	3.4	V	
Signal Rate per Channel	B	2.5		10.3125	GB/s	Note 1
Power Supply Noise Ripple Susceptibility	PSNR			50	mVpp	Note 2
Bit Error Ratio			10 ⁻¹²			Note 3
Control Input Voltage High	V _{ih}	2		V _{cc} +0.3	V	
Control Input Voltage Low	V _{il}	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate				400	kHz	
Differential Data Input / Output Load	Z _d		100		Ohms	
Standard Cable Lengths		3		100	m	Note 4

Note 1. Lane speed up to 12.5-Gbps is available upon customer requests.

Note 2. Power supply noise is defined as peak-to-peak noise amplitude over 1K to 15 MHz frequency range at host supply side by the recommended power supply filter for module. See Section 10 for the recommended power supply filter.

Note 3. Bit-Error-Rate (BER) is tested with PRBS 2³¹-1 pattern.

Note 4. Longer cable length (up to 150-m) is available upon customer request.



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Electrical characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Transceiver Power Consumption	P			1.5	W	
Transceiver Power Supply Current	I_{cc}			420	mA	
Transceiver Power-On Initialization Time				2000	ms	Note 1

Transmitter Electrical characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Input Differential Peak-to-Peak Voltage Swing	V_{DIFF}	200		1600	mVpp	
Differential Input Return Loss	Per IEEE 802.3ba, Section 86A.4.1.1				dB	Note 2
Differential to Common Mode Input Return Loss		10			dB	Note 2
J2 Jitter Tolerance	J_{t2}	0.17			UI	
J9 Jitter Tolerance	J_{t9}	0.29			UI	
Eye Mask Coordinates: X1, X2; Y1, Y2.		Specification Value 0.11, 0.31; 95, 350.			UI; mV	Note 3

Receiver Electrical characteristics

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTE
Data Output Differential Peak-to-Peak Voltage Swing	V_{DIFF}	200		900	mVpp	Note 4
Output Transition Time 20% to 80%		28			ps	
Differential Output Return Loss	Per IEEE 802.3ba, Section 86A.4.2.1				dB	Note 2
Common Mode Output Return Loss	Per IEEE 802.3ba, Section 86A.4.2.2				dB	Note 2
Output Total Jitter				62	ps	
J2 Jitter Output	J_{o2}			0.42	UI	
J9 Jitter Output	J_{o9}			0.65	UI	
Eye Mask Coordinates: X1, X2; Y1, Y2.		Specification Value 0.29, 0.5; 150, 425.			UI; mV	Note 3

Note 1. "Initialization Time" is the time from when the supply voltages reach and remain above the minimum "Recommended Operating Conditions" to the time when the module enables TWS access. The module at that point is fully functional.

Note 2. 10M to 11.1 GHz according to IEEE 802.3ba specification.

Note 3. Hit ratio= 5×10^{-5} per sample.

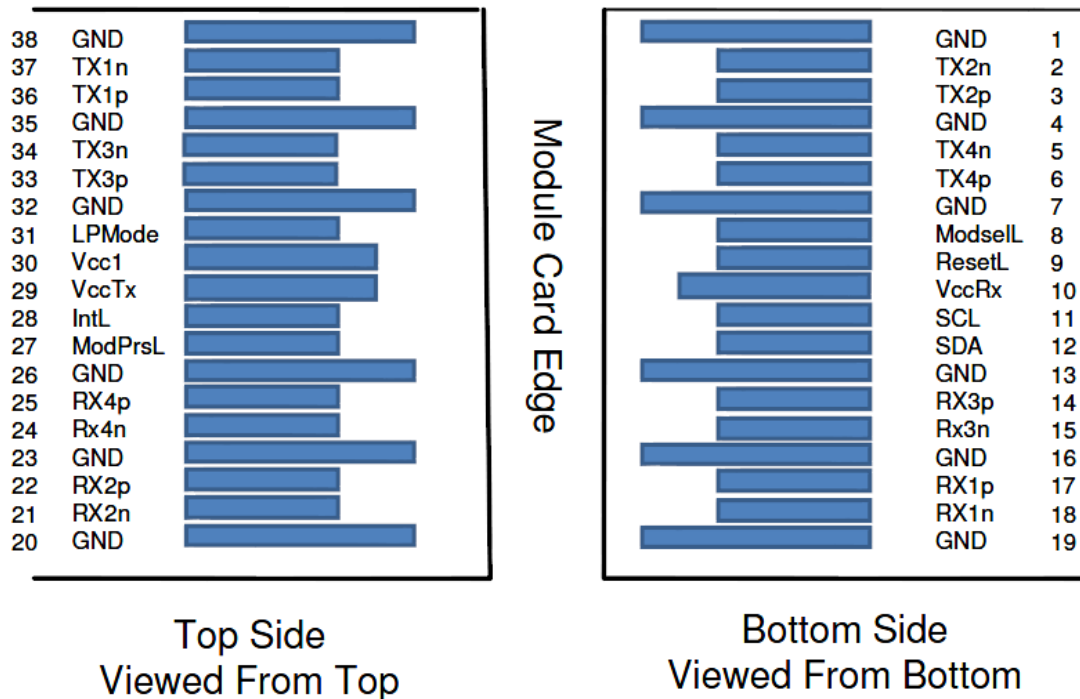
Note 4. AC-Coupled with 100Ω differential output impedance.

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Pad assignment and Description



PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
1		GND	Ground	1	Note 1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	Note 1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	Note 1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	Note 2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	Note 2
14	CML-O	Rx3p	Receiver Non- Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	Note 1
17	CML-O	Rx1p	Receiver Non- Inverted Data Output	3	



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PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	Note 1
20		GND	Ground	1	Note 1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2P	Receiver Non- Inverted Data Output	3	
23		GND	Ground	1	Note 1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non- Inverted Data Output	3	
26		GND	Ground	1	Note 1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29	LVC MOS-I/O	Vcc Tx	+3.3V Power Supply transmitter	2	Note 2
30		Vcc1	+3.3V Power Supply	2	Note 2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	Note 1
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	Note 1
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	Note 1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

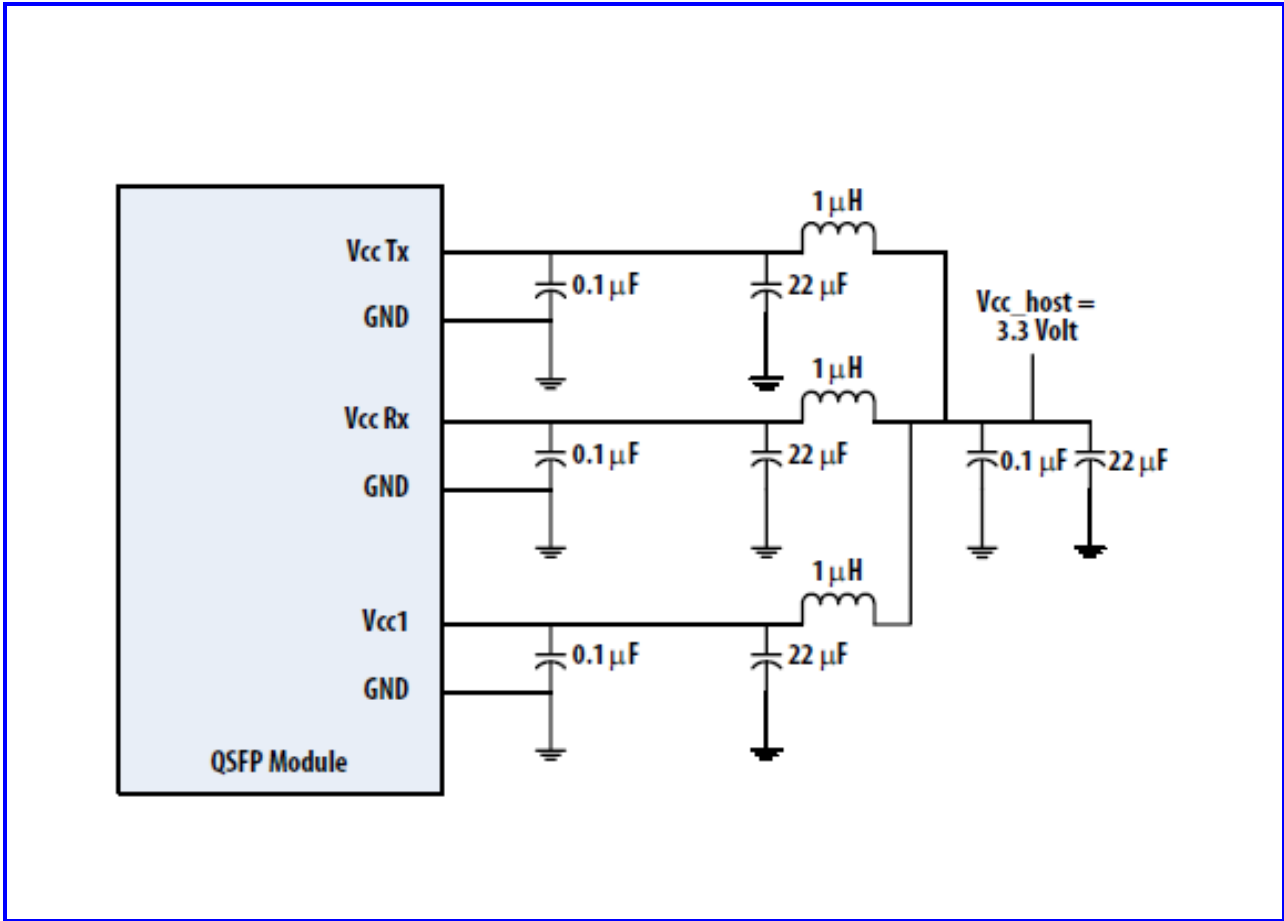
Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

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Host board power supply circuit

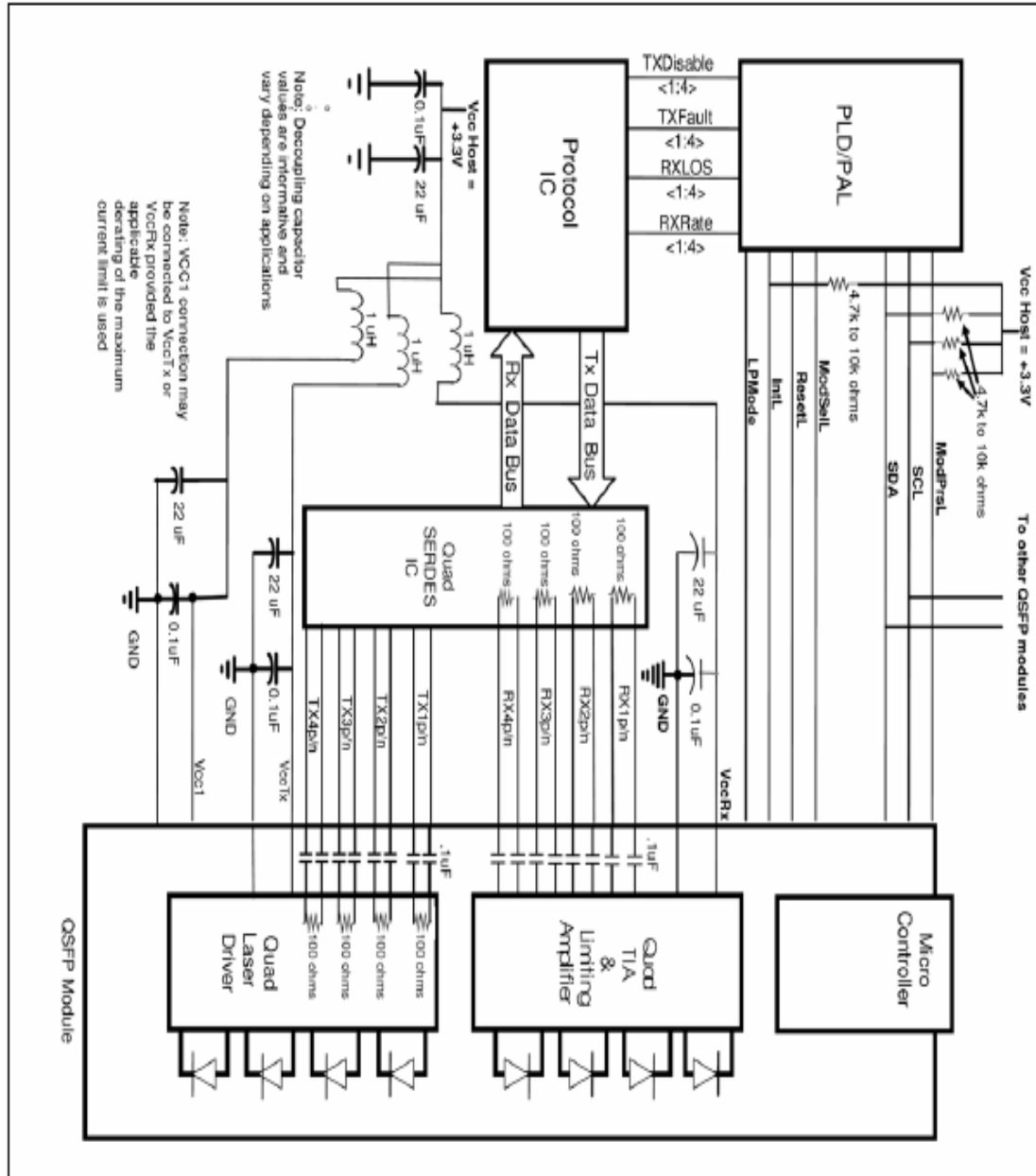


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Recommended Interface circuit

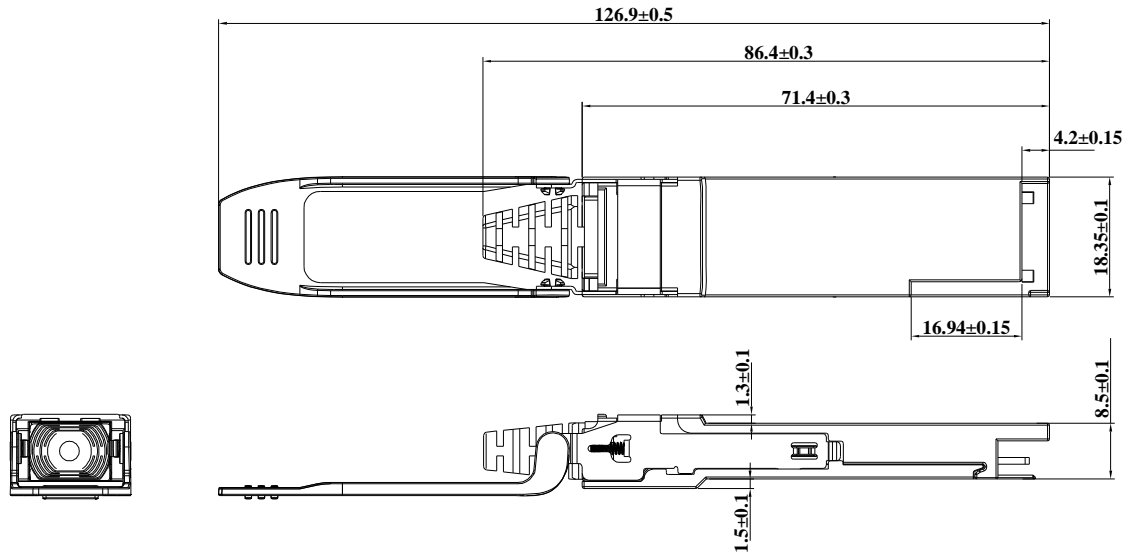


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Dimensions

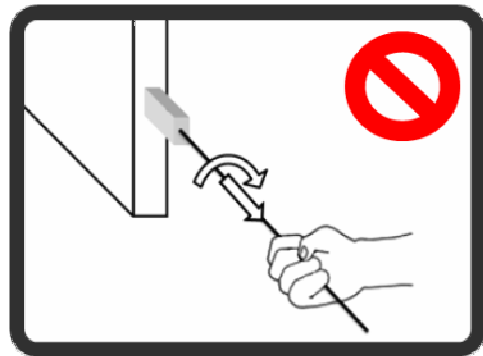
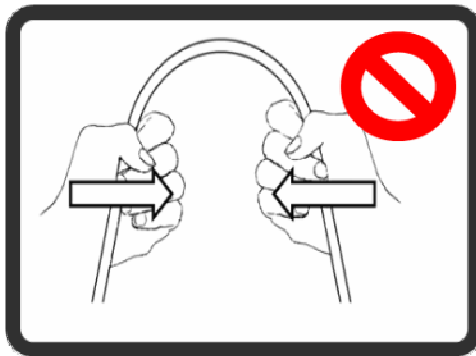


Unit: mm

All Dimensions are ±0.20mm Unless Otherwise Specified

Handling

Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Put the product in an even and stable location. If the product falls down or drops, it may cause an injury or malfunction. The cable must not be subject to extreme bends during installation or while in operation. If you bend the cable at a radius less than the cable minimum bend radius, then the cable may get damaged. Don't twist or pull by force ends of the cable, which might cause malfunction. In addition, the bending direction should be perpendicular to the flat surface of the ribbon cable. Please do not bend or kink the cable in lateral directions of flat surface of the ribbon.





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Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP+ SFF-8436 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.

